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*****
9158 Sun Sep 27 09:37:18 2015
new/usr/src/uts/intel/asm/atomic.h
6263 add missing cc clobbers to intel atomic inlines
*****
1 /*
2  * CDDL HEADER START
3  *
4  * The contents of this file are subject to the terms of the
5  * Common Development and Distribution License, Version 1.0 only
6  * (the "License"). You may not use this file except in compliance
7  * with the License.
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17 * fields enclosed by brackets "[]" replaced with your own identifying
18 * information: Portions Copyright [yyyy] [name of copyright owner]
19 *
20 * CDDL HEADER END
21 */
22 /*
23  * Copyright 2005 Sun Microsystems, Inc. All rights reserved.
24  * Use is subject to license terms.
25  * Copyright 2014 Nexenta Systems, Inc. All rights reserved.
26  * Copyright 2015 Josef 'Jeff' Sipek <jeffpc@josefsipek.net>
27 #endif /* ! codereview */
28 */

30 #ifndef _ASM_ATOMIC_H
31 #define _ASM_ATOMIC_H

33 #include <sys/ccompile.h>
34 #include <sys/types.h>

36 #ifdef __cplusplus
37 extern "C" {
38 #endif

40 #if !defined(__lint) && defined(__GNUC__)

42 /* BEGIN CSTYLED */
43 /*
44  * This file contains a number of static inline functions implementing
45  * various atomic variable functions. Note that these are *not* all of the
46  * atomic_* functions as defined in usr/src/uts/common/sys/atomic.h. All
47  * possible atomic_* functions are implemented in usr/src/common/atomic in
48  * pure assembly. In the absence of an identically named function in this
49  * header file, any use of the function will result in the compiler emitting
50  * a function call as usual. On the other hand, if an identically named
51  * function exists in this header as a static inline, the compiler will
52  * inline its contents and the linker never sees the symbol reference. We
53  * use this to avoid implementing some of the more complex and less used
54  * functions and instead falling back to function calls. Note that in some
55  * cases (e.g., atomic_inc_64) we implement a static inline only on AMD64
56  * but not i386.
57  */

59 /*
60  * Instruction suffixes for various operand sizes (assuming AMD64)
61  */

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62 #define SUF_8          "b"
63 #define SUF_16         "w"
64 #define SUF_32         "l"
65 #define SUF_64         "q"

67 #if defined(__amd64)
68 #define SUF_LONG        SUF_64
69 #define SUF_PTR         SUF_64
70 #define __ATOMIC_OP64(...) __ATOMIC_OPXX(__VA_ARGS__)
71 #elif defined(__i386)
72 #define SUF_LONG        SUF_32
73 #define SUF_PTR         SUF_32
74 #define __ATOMIC_OP64(...)
75 #else
76 #error "port me"
77 #endif

79 #if defined(__amd64) || defined(__i386)

81 #define __ATOMIC_OPXX(fxn, type, op)
82 extern __GNU_INLINE void
83 fxn(volatile type *target)
84 {
85     __asm__ volatile (
86         "lock; " op " %0"
87         : "+m" (*target)
88         : /* no inputs */
89         : "cc");
90     : "+m" (*target));
91 }

92 __ATOMIC_OPXX(atomic_inc_8,      uint8_t,  "inc" SUF_8)
93 __ATOMIC_OPXX(atomic_inc_16,     uint16_t, "inc" SUF_16)
94 __ATOMIC_OPXX(atomic_inc_32,     uint32_t, "inc" SUF_32)
95 __ATOMIC_OPXX(atomic_inc_64,     uint64_t, "inc" SUF_64)
96 __ATOMIC_OPXX(atomic_inc_uchar,  uchar_t,  "inc" SUF_8)
97 __ATOMIC_OPXX(atomic_inc_ushort, ushort_t, "inc" SUF_16)
98 __ATOMIC_OPXX(atomic_inc_uint,  uint_t,   "inc" SUF_32)
99 __ATOMIC_OPXX(atomic_inc_ulong,  ulong_t,  "inc" SUF_LONG)

101 __ATOMIC_OPXX(atomic_dec_8,      uint8_t,  "dec" SUF_8)
102 __ATOMIC_OPXX(atomic_dec_16,     uint16_t, "dec" SUF_16)
103 __ATOMIC_OPXX(atomic_dec_32,     uint32_t, "dec" SUF_32)
104 __ATOMIC_OPXX(atomic_dec_64,     uint64_t, "dec" SUF_64)
105 __ATOMIC_OPXX(atomic_dec_uchar,  uchar_t,  "dec" SUF_8)
106 __ATOMIC_OPXX(atomic_dec_ushort, ushort_t, "dec" SUF_16)
107 __ATOMIC_OPXX(atomic_dec_uint,  uint_t,   "dec" SUF_32)
108 __ATOMIC_OPXX(atomic_dec_ulong,  ulong_t,  "dec" SUF_LONG)

110 #undef __ATOMIC_OPXX

112 #define __ATOMIC_OPXX(fxn, type1, type2, op, reg)
113 extern __GNU_INLINE void
114 fxn(volatile type1 *target, type2 delta)
115 {
116     __asm__ volatile (
117         "lock; " op " %1,%0"
118         : "+m" (*target)
119         : "i" reg (delta)
120         : "cc");
121     : "i" reg (delta));
122 }

123 __ATOMIC_OPXX(atomic_add_8,      uint8_t,  int8_t,  "add" SUF_8,  "q")
124 __ATOMIC_OPXX(atomic_add_16,     uint16_t, int16_t, "add" SUF_16, "r")
125 __ATOMIC_OPXX(atomic_add_32,     uint32_t, int32_t,  "add" SUF_32, "r")

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126 __ATOMIC_OP64(atomic_add_64,    uint64_t, int64_t,    "add" SUF_64,    "r")
127 __ATOMIC_OPXX(atomic_add_char,  uchar_t,  signed char, "add" SUF_8,    "q")
128 __ATOMIC_OPXX(atomic_add_short, ushort_t,  short,    "add" SUF_16,   "r")
129 __ATOMIC_OPXX(atomic_add_int,   uint_t,   int,        "add" SUF_32,   "r")
130 __ATOMIC_OPXX(atomic_add_long,  ulong_t,   long,       "add" SUF_LONG, "r")

132 /*
133  * We don't use the above macro here because atomic_add_ptr has an
134  * inconsistent type. The first argument should really be a 'volatile void
135  * ***'.
136  */
137 extern __GNU_INLINE void
138 atomic_add_ptr(volatile void *target, ssize_t delta)
139 {
140     volatile void **tmp = (volatile void **)target;

142     __asm__ __volatile__(
143         "lock; add" SUF_PTR " %1,%0"
144         : "+m" (*tmp)
145         : "ir" (delta)
146         : "cc");
147     : "ir" (delta);
148 }
149
150 unchanged portion omitted
```