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*****
9842 Fri Apr 4 13:25:23 2014
new/usr/src/uts/i86pc/io/pcplusmp/apic_regops.c
patch enum
*****
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19 * CDDL HEADER END
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21 /*
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24 */

26 #include <sys/cpuvar.h>
27 #include <sys/psm.h>
28 #include <sys/archsystem.h>
29 #include <sys/apic.h>
30 #include <sys/sunddi.h>
31 #include <sys/ddi_impldefs.h>
32 #include <sys/mach_intr.h>
33 #include <sys/sysmacros.h>
34 #include <sys/trap.h>
35 #include <sys/x86_archext.h>
36 #include <sys/privregs.h>
37 #include <sys/psm_common.h>

39 /* Function prototypes of local apic and X2APIC */
40 static uint64_t local_apic_read(uint32_t reg);
41 static void local_apic_write(uint32_t reg, uint64_t value);
42 static int get_local_apic_pri(void);
43 static void local_apic_write_task_reg(uint64_t value);
44 static void local_apic_write_int_cmd(uint32_t cpu_id, uint32_t cmd1);
45 static uint64_t local_x2apic_read(uint32_t msr);
46 static void local_x2apic_write(uint32_t msr, uint64_t value);
47 static int get_local_x2apic_pri(void);
48 static void local_x2apic_write_task_reg(uint64_t value);
49 static void local_x2apic_write_int_cmd(uint32_t cpu_id, uint32_t cmd1);

51 /*
52 * According to the X2APIC specification:
53 *
54 * xAPIC global enable    X2APIC enable    Description
55 * (IA32_APIC_BASE[11])  (IA32_APIC_BASE[10])
56 * -----
57 *      0                  0          APIC is disabled
58 *      0                  1          Invalid
59 *      1                  0          APIC is enabled in xAPIC mode
60 *      1                  1          APIC is enabled in X2APIC mode
61 * -----

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62 */
63 int    x2apic_enable = 1;
64 enum apic_mode apic_mode = LOCAL_APIC; /* Default mode is Local APIC */
64 int    apic_mode = LOCAL_APIC; /* Default mode is Local APIC */

66 /* Uses MMIO (Memory Mapped IO) */
67 static apic_reg_ops_t local_apic_regops = {
68     local_apic_read,
69     local_apic_write,
70     get_local_apic_pri,
71     local_apic_write_task_reg,
72     local_apic_write_int_cmd,
73     apic_send_EOI,
74 };
_____unchanged_portion_omitted_

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new/usr/src/uts/i86pc/sys/apic.h

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21 /*
22 * Copyright (c) 1993, 2010, Oracle and/or its affiliates. All rights reserved.
23 */

25 /*
26 * Copyright (c) 2010, Intel Corporation.
27 * All rights reserved.
28 */

30 #ifndef _SYS_APIC_APIC_H
31 #define _SYS_APIC_APIC_H

33 #include <sys/psm_types.h>
34 #include <sys/avintr.h>
35 #include <sys/pci.h>

37 #ifdef __cplusplus
38 extern "C" {
39 #endif

41 #include <sys/psm_common.h>

43 #define APIC_PCPLUSMP_NAME      "pcplusmp"
44 #define APIC_APIX_NAME         "apix"

46 #define APIC_IO_ADDR           0xfec00000
47 #define APIC_LOCAL_ADDR       0xfee00000
48 #define APIC_IO_MEMLEN        0xf
49 #define APIC_LOCAL_MEMLEN     0xffff

51 /* Local Unit ID register */
52 #define APIC_LID_REG           0x8

54 /* I/o Unit Version Register */
55 #define APIC_VERS_REG          0xc

57 /* Task Priority register */
58 #define APIC_TASK_REG          0x20

60 /* EOI register */
61 #define APIC_EOI_REG           0x2c
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63 /* Remote Read register */
64 #define APIC_REMOTE_READ      0x30

66 /* Logical Destination register */
67 #define APIC_DEST_REG         0x34

69 /* Destination Format register */
70 #define APIC_FORMAT_REG       0x38

72 /* Spurious Interrupt Vector register */
73 #define APIC_SPUR_INT_REG     0x3c

75 /* Error Status Register */
76 #define APIC_ERROR_STATUS     0xa0

78 /* Interrupt Command registers */
79 #define APIC_INT_CMD1         0xc0
80 #define APIC_INT_CMD2         0xc4

82 /* Local Interrupt Vector registers */
83 #define APIC_CMCI_VECT        0xbc
84 #define APIC_THERM_VECT       0xcc
85 #define APIC_PCINT_VECT       0xd0
86 #define APIC_INT_VECT0        0xd4
87 #define APIC_INT_VECT1        0xd8
88 #define APIC_ERR_VECT         0xdc

90 /* IPL for performance counter interrupts */
91 #define APIC_PCINT_IPL        0xe
92 #define APIC_LVT_MASK         0x10000 /* Mask bit (16) in LVT */

94 /* Initial Count register */
95 #define APIC_INIT_COUNT       0xe0

97 /* Current Count Register */
98 #define APIC_CURR_COUNT        0xe4
99 #define APIC_CURR_ADD          0x39 /* used for remote read command */
100 #define CURR_COUNT_OFFSET     (sizeof (int32_t) * APIC_CURR_COUNT)

102 /* Divider Configuration Register */
103 #define APIC_DIVIDE_REG        0xf8

105 /* Various mode for local APIC. Modes are mutually exclusive */
106 enum apic_mode {
107     APIC_IS_DISABLED,
108     APIC_MODE_NOTSET,
109     LOCAL_APIC,
110     LOCAL_X2APIC,
111 };
106 #define APIC_IS_DISABLED      0x0
107 #define APIC_MODE_NOTSET      0x1
108 #define LOCAL_APIC            0x2
109 #define LOCAL_X2APIC          0x3

113 /* x2APIC SELF IPI Register */
114 #define APIC_X2APIC_SELF_IPI  0xfc

116 /* General x2APIC constants used at various places */
117 #define APIC_SVR_SUPPRESS_BROADCAST_EOI 0x1000
118 #define APIC_DIRECTED_EOI_BIT          0x1000000

120 /* IRR register */
121 #define APIC_IRR_REG           0x80

123 /* ISR register */
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124 #define APIC_ISR_REG          0x40
126 #define APIC_IO_REG          0x0
127 #define APIC_IO_DATA        0x4
128 #define APIC_IO_EOI          0x10

130 /* Bit offset of APIC ID in LID_REG, INT_CMD and in DEST_REG */
131 #define APIC_ID_BIT_OFFSET    24
132 #define APIC_ICR_ID_BIT_OFFSET 24
133 #define APIC_LDR_ID_BIT_OFFSET 24

135 /*
136  * Choose between flat and clustered models by writing the following to the
137  * FORMAT_REG. 82489 DX documentation seemed to suggest that writing 0 will
138  * disable logical destination mode.
139  * Does not seem to be in the docs for local APICs on the processors.
140  */
141 #define APIC_FLAT_MODEL        0xFFFFFFFFUL
142 #define APIC_CLUSTER_MODEL    0x0FFFFFFF

144 /*
145  * The commands which follow are window selectors written to APIC_IO_REG
146  * before data can be read/written from/to APIC_IO_DATA
147  */

149 #define APIC_ID_CMD           0x0
150 #define APIC_VERS_CMD        0x1
151 #define APIC_RDT_CMD         0x10
152 #define APIC_RDT_CMD2        0x11

154 #define APIC_INTEGRATED_VERS 0x10 /* 0x10 & above indicates integrated */
155 #define IOAPIC_VER_82489DX   0x01 /* Version ID: 82489DX External APIC */

157 #define APIC_INT_SPURIOUS    -1

159 #define APIC_IMCR_P1         0x22 /* int mode conf register port 1 */
160 #define APIC_IMCR_P2         0x23 /* int mode conf register port 2 */
161 #define APIC_IMCR_SELECT    0x70 /* select imcr by writing into P1 */
162 #define APIC_IMCR_PIC        0x0 /* selects PIC mode (8259-> BSP) */
163 #define APIC_IMCR_APIC       0x1 /* selects APIC mode (8259->APIC) */

165 #define APIC_CT_VECT         0x4ac /* conf table vector */
166 #define APIC_CT_SIZE         1024 /* conf table size */

168 #define APIC_ID              'MPAT' /* conf table signature */

170 #define VENID_AMD             0x1022
171 #define DEVID_8131_IOAPIC    0x7451
172 #define DEVID_8132_IOAPIC    0x7459

174 #define IOAPICS_NODE_NAME    "ioapics"
175 #define IOAPICS_CHILD_NAME   "ioapic"
176 #define IOAPICS_DEV_TYPE     "ioapic"
177 #define IOAPICS_PROP_VENID   "vendor-id"
178 #define IOAPICS_PROP_DEVID   "device-id"

180 #define IS_CLASS_IOAPIC(b, s, p) \
181     ((b) == PCI_CLASS_PERIPH && (s) == PCI_PERIPH_PIC && \
182      ((p) == PCI_PERIPH_PIC_IF_IO_APIC || \
183       (p) == PCI_PERIPH_PIC_IF_IOX_APIC))

185 /*
186  * These macros are used in frequently called routines like
187  * apic_intr_enter().
188  */
189 #define X2APIC_WRITE(reg, v) \

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190     wrmsr((REG_X2APIC_BASE_MSR + (reg >> 2)), v)

192 #define LOCAL_APIC_WRITE_REG(reg, v) \
193     apicadr[reg] = v

195 /*
196  * MP floating pointer structure defined in Intel MP Spec 1.1
197  */
198 struct apic_mpfps_hdr {
199     uint32_t    mpfps_sig; /* _MP_ (0x5F4D505F) */
200     uint32_t    mpfps_mpct_paddr; /* paddr of MP configuration tbl */
201     uchar_t    mpfps_length; /* in paragraph (16-bytes units) */
202     uchar_t    mpfps_spec_rev; /* version number of MP spec */
203     uchar_t    mpfps_checksum; /* checksum of complete structure */
204     uchar_t    mpfps_featinfo1; /* mp feature info bytes 1 */
205     uchar_t    mpfps_featinfo2; /* mp feature info bytes 2 */
206     uchar_t    mpfps_featinfo3; /* mp feature info bytes 3 */
207     uchar_t    mpfps_featinfo4; /* mp feature info bytes 4 */
208     uchar_t    mpfps_featinfo5; /* mp feature info bytes 5 */
209 };
_____unchanged_portion_omitted_____

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